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Remarks

Claims 1-20 are active in the application.

I. CLAIM REJECTIONS UNDER 35 USC § 102(b)

Claims 1, 2, 4, 6, 7 and 10 are rejected under 35 USC § 102(b) as being anticipated by United States patent no. 5,986,885 of Wyland. The applicants respectfully traverse the rejection on the grounds that Wyland does not disclose every element of claims 1, 2, 4, 6, 7 and 10 as now amended.

Wyland's Figure 6 shows die 30 attached to first circuitry metallizations 61 by flip-chip bonding. The applicants respectfully submit that Wyland's first circuitry metallizations do not constitute a mounting pad in the sense in which the term is used in the application, i.e., a pad to which a semiconductor die is attached with the major surface of the die in contact with the mounting pad. The applicants have amended claim 1 accordingly. The applicants respectfully submit that Wyland neither teaches nor suggests "a conductive mounting pad for attachment of the die with a major surface of the die in contact therewith", as recited in claim 1 as now amended. Accordingly, the applicants respectfully submit that claim 1 is allowable.

The applicants further submit that claims 2-10, which depend on claim 1, are allowable because of their dependence on claim 1.

With regard to claim 6, the official action alleges that Wyland discloses a bonding pad, citing "(right side, Figure 6) (31) (Col. 7, lines 19 - 21)." The applicants respectfully disagree. Wyland's bonding pads 31 are described at col. 6, lines 48-49, as being "on the surface of die 30" and are clearly shown that way in Figure 6. The passage of Wyland's disclosure cited in the official action additionally describes the bonding pads 31 as being attached to first circuitry metallizations 61 by conventional means such as solder 59. Wyland's bonding pads 31 are shown in Figure 6 as being separated from the major surface of substrate 60 by solder 59. Thus, the applicants respectfully submit that Wyland's bonding pads 31 are not part of the semiconductor package. The applicants further submit that Wyland's bonding pads 31 cannot accurately be described as being

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"on the one of the major surfaces [of the planar substrate]". Therefore, the applicants respectfully submit that Wyland does not disclose "a bonding pad located on the one of the major surfaces" as recited in claim 6 and that claim 6 is allowable for this additional reason.

Claims 11, 12, 16 and 17 are rejected under 35 USC § 102(b) as being anticipated by United States patent no. 6,084,295 of Horiuchi et al. (*Horiuchi*). The applicants respectfully traverse the rejection on the grounds that Horiuchi does not disclose every element of claims 11, 12, 16 and 17.

The official action alleges that Horiuchi discloses "a conductive "mounting pad" (upper surface) (Figures 1, 7(a) and 7(c)) (Col. 6, line 64 Col. 7, line 2) located on one of the major surfaces ... a conductive interconnecting element (42) extending through the substrate and electrically connecting the mounting pad and the connecting pad (Col. 6, line 64 - Col. 7, line 2); and a semiconductor die (10) (Figure 1) attached to the mounting pad."

In the embodiment shown in Horiuchi's Figure 1, a die 10 is attached to the major surface of a substrate 5. The applicants have been unable to find anything in Horiuchi's description of Figure 1 that teaches or suggests that the portion of the major surface of the substrate underlying the die is conducting. In Horiuchi's Figure 1, the vias underlying the die are given a reference numeral (16) different from that (18) assigned to the vias to which bonding wires are attached. Thus, there is nothing in Horiuchi's disclosure that teaches or suggests that vias 16 underlying the die are structured similarly to the vias 18 to which bonding wires are attached and that are shown in detail in Figure 2. Moreover, the applicants have been unable to find anything in Horiuchi's disclosure that teaches or suggests that any conductive structure exists located on the major surface of substrate 5 to which die 10 is attached. Since none of the vias 16 extends over the major surface of substrate 5 underneath die 10, the applicants respectfully submit that the embodiment of Horiuchi's semiconductor device does not comprise "a conductive mounting pad located on one of the major surfaces;" as recited in claim 11.

Horiuchi's Figures 7(a) and 7(b) show variations on the circuit board structure

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shown in Figure 1. In particular, these Figures show different structures of the vias 18 to which the bonding wires are attached (see Figures 7(a) and 7(b) and col. 6, line 67-col. 7, line 1). The applicants have been unable to find anything in Horiuchi's disclosure that teaches or suggests that the vias 16 underlying die 10 could be structured similarly to the vias 42 shown in Figures 7(a) and 7(b). Moreover, even if the vias 16 underlying die 10 were structured similarly to the vias 42 shown in Figures 7(a) and 7(b), the resulting structure would not comprise "a conductive mounting pad *located on* one of the major surfaces [of a substantially planar substrate]." No part of the vias 42 extends over the major surface of substrate 5 on which the die 10 is mounted. Additionally, in the variations shown in Figures 7(a) and 7(b), the solder bumps 12 are located on the end surfaces of the vias 42 that extend through the substrate 5. No part of the vias 42 extends over the major surface of substrate 5 opposite that on which the die 10 is mounted. The variations shown in Figures 7(a) and 7(b) therefore additionally lack "a conductive connecting pad located on the other of the major surfaces," as recited in claim 11.

Accordingly, the applicants respectfully submit that Horiuchi cannot accurately be said to disclose at least "a conductive mounting pad located on one of the major surfaces [of a substantially planar substrate]", as recited in claim 11. The applicants therefore submit that Horiuchi does not disclose every element of claim 11, and that claim 11 is therefore allowable.

The applicants further submit that claims 12-20, which depend on claim 11, are also allowable because of their dependence on claim 11.

II. CLAIM REJECTIONS UNDER 35 USC § 103(a)

1. Claims 3 and 8

Claims 3 and 8 are rejected under 35 USC §103(a) as being unpatentable over Wyland as applied to claims 1, 2, 4, 6, 7 and 10 in view of *Innovative PCB Reinforcement*, ELECTRONIC PACKAGING AND PRODUCTION, 1 (February 1997) (the *Article*). The applicants traverse the rejection on the grounds that the official action does not set forth a prima facie case of obviousness that complies with the requirements of

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MPEP § 2143.

First, the applicants respectfully submit that Wyland's semiconductor package, modified as proposed in the official action, would still lack a mounting pad, for the reason set forth above with reference to claim 1. Accordingly, the applicants respectfully submit that the proposed combination of references does not teach or suggest every element of claims 3 and 8.

Second, the official action states:

[I]t would have been obvious to one of ordinary skill in the art at the time of the invention to combine the disclosures of Electronic Packaging and Technology with Wyland to obtain a device with increased reliability and reduced fatigue at joints (p. 1, left column, 5th para.).

The Article discloses mounting thin, small outline integrated circuit packages (TSOPs) on a multilayer reinforced epoxy laminate printed circuit board. The TSOPs are composed of a semiconductor die attached to a metal lead frame. The die and part of the lead frame are encapsulated. Portions of the lead frame remote from the die are attached to the printed circuit board by solder. The use of an epoxy laminate as the material of the printed circuit board was apparently motivated by the need for the printed circuit board to match the coefficient of thermal expansion of the TSOPs to increase the reliability of solder connections between the TSOPs and the printed circuit board.

The structure of Wyland's device is different: a semiconductor die 30 is flip-chip mounted on first circuitry metallizations 61 located on the surface of a substrate 60.

The applicants respectfully submit that the person of ordinary skill in the art would appreciate that the thermal expansion considerations of Wyland's semiconductor device are so different from those of a TSOP attached to a printed circuit board that such person consider any teaching set forth in the Article with respect to the printed circuit board material as inapplicable to choosing the substrate material of Wyland's semiconductor package. Accordingly, the applicants respectfully submit that such person would lack a motivation to make the combination of references proposed in the official action.

The applicants therefore respectfully submit that the rejection of claims 3 and 8 is

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improper because the rationale set forth in the official action for combining the cited references does not meet the requirements set forth in MPEP § 2143. The applicants therefore respectfully request that the rejection be withdrawn.

2. Claims 5 and 10

Claims 5 and 10 are rejected under 35 USC § 103(a) as being unpatentable over Wyland, as applied to Claims 1, 2, 4, 6, 7 and 10, in view of Wilson et al., HANDBOOK OF MULTILEVEL METALLIZATION FOR INTEGRATED CIRCUITS, 868 – 872, Noyes Publ., Westwood, New Jersey, (1993) (the *Handbook*). The applicants traverse the rejection on the grounds that the official action does not set forth a prima facie case of obviousness that complies with the requirements of MPEP § 2143.

First, the applicants respectfully submit that Wyland's device, modified as proposed in the official action, would still lack a mounting pad for the reason set forth above with reference to claim 1. Accordingly, the applicants respectfully submit that the proposed combination of references does not teach or suggest every element of claims 5 and 10.

Second, the official action states:

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Wilson et al. with Wyland to reduce costs (p. 868, lines 11 - 12) and reduce signal delays (p. 872, Figure 10).

The cited passage of the *Handbook* describes the advantages of CVD tungsten in integrated circuits with three or more levels of metallization (p.868, line 8). The substrate 60 of Wyland's semiconductor device, on the other hand, has no more than two levels of metallization. Moreover, the portion of Wyland's semiconductor device to which the official action proposes to apply the teachings of the *Handbook* is the substrate of a semiconductor package. The applicants respectfully submit that the substrate of a semiconductor package cannot accurately be referred to as an integrated circuit. Accordingly, the applicants respectfully submit that the person of ordinary skill in the art would regard the teaching set forth in the *Handbook* with respect to the material of the interlayer plugs of an integrated circuit with three or more levels of metallization

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inapplicable to the choice of material of the through holes 61 of Wyland's semiconductor package. Accordingly, the applicants respectfully submit that such person would lack a motivation to make the combination of references proposed in the official action.

Referring to the motivations proposed in the official action, the applicants have been unable to find any teaching in the Handbook with regard to tungsten having a cost advantage in an application other than an integrated circuit with three or more levels of metallization. Additionally, it is not clear from Figure 10 whether the data disclosed therein relates to interlayer plugs or to on-layer traces. The distance scales suggest the latter. Finally, it is not clear from Figure 10 that tungsten actually provides the advantage of reduced signal delays, as asserted in the official action.

Accordingly, the applicants respectfully submit that the motivation set forth in the official action for combining the cited references does not meet the requirements set forth in MPEP § 2143.

Therefore, the applicants respectfully submit that the rejection of claims 5 and 10 is improper because the prima facie case of obviousness set forth in the official action does not meet the requirements set forth in MPEP § 2143. The applicants therefore respectfully request that the rejection be withdrawn.

3. Claim 9

Claim 9 is rejected under 35 USC § 103(a) as being unpatentable over Wyland as applied to Claims 1, 2, 4, 6, 7 and 10 in view of United States patent no. 6,620,720 of Moyer et al. (*Moyer*). The applicants traverse the rejection on the grounds that the official action does not set forth a prima facie case of obviousness that complies with the requirements of MPEP § 2143.

First, the applicants respectfully submit that Wyland's device, modified as proposed in the official action, would still lack a mounting pad for the reason set forth above with reference to claim 1. Accordingly, the applicants respectfully submit that the proposed combination of references does not teach or suggest every element of claim 9.

Second, the official action states:

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Wyland discloses (Col. 7, lines 31 - 39) that the mounting pad (61), and the connecting pad (63) are composed of copper, but does not disclose that the bond pad is composed of copper. Moyer et al. disclose (Col. 2, lines 48 - 49) that a copper contact (bond) pad (13) (Figure 1) is formed on the silicon substrate for either wire bonding or solder bump bonding.

The applicants respectfully submit that Wyland's semiconductor package, modified as proposed in the official action, additionally lacks a copper bonding pad located on the one of the major surfaces [of the substantially planar substrate] as claimed in claim 9. As noted above in the discussion of claim 6 on which claim 9 depends, Wyland's bonding pad 31 is located on the die 30 and cannot therefore be accurately be described as being "located on the one of the major surfaces [of the substantially planar substrate]". Accordingly, the applicants respectfully submit that the facie case of obviousness set forth in the official action does not comply with the requirements of MPEP § 2143 because the proposed combination of references does not teach or suggest all the claim limitations.

Third, the official action additionally states:

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Moyer et al. with Wyland to provide a contact (bond) pad of low cost and high conductivity (Moyer et al., Col. 1, lines 41 - 43).

In the lines following the passage of Moyer's disclosure cited in the official action, Moyer discloses some of the many difficulties of using copper in integrated circuits. Moyer discloses a solution to the problems of using copper to form the bonding pads of an integrated circuit. Moyer's solution involves the deposition of several additional layers over the copper bonding pad. The applicants respectfully submit that the person of ordinary skill in the art would appreciate that the main motivation for adopting copper interconnects in integrated circuits, namely, maintaining low-resistance connections despite ever-decreasing feature sizes, does not apply to selecting the material of the bonding pads of Wyland's semiconductor package. The applicants respectfully submit that this absence of a motivation to use copper, together with Moyer's disclosure of the additional complexity of using copper, means that such person would have no motivation to adopt the teaching set forth in Moyer's disclosure with respect to the

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material of the bonding pads of the packaging device.

Accordingly, the applicants respectfully submit that the rejection of claim 9 is improper because the prima facie case of obviousness set forth in the official action does not comply with the requirements of MPEP § 2143. The applicants therefore respectfully request that the rejection be withdrawn.

4. Claims 13 and 18

Claims 13 and 18 are rejected under 35 USC § 103(a) as being unpatentable over Horiuchi as applied to Claims 11, 12, 16, and 17, in view of the Article. The applicants traverse this rejection on the grounds that the prima facie case of obviousness set forth in the official action does not comply with the requirements of MPEP § 2143.

First, the applicants respectfully submit that Horiuchi's device, modified as proposed in the official action, would still lack a mounting pad for the reasons set forth above with reference to claim 11. Accordingly, the applicants respectfully submit that the proposed combination of references does not teach or suggest every element of claims 13 and 18.

Second, the official action states:

[I]t would have been obvious to one of ordinary skill in the art at the time of the invention to combine the disclosures of Electronic Packaging and Technology with Horiuchi et al. to obtain a device with increased reliability and reduced fatigue at joints (p. 1, left column, 5th para.).

Second, the disclosure of the Article is described above with reference to claims 3 and 8. The structure of Horiuchi's device package is different that of the TSOPs discussed in the Article: semiconductor die 10 is attached directly to the surface of substrate 5.

The applicants respectfully submit that the person of ordinary skill in the art would appreciate that the thermal expansion considerations of Horiuchi's device package are so different from those of a TSOP attached to a printed circuit board that such person would consider any teaching set forth in the Article with respect to printed circuit board material as inapplicable to choosing the substrate material of Horiuchi's device package.

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Accordingly, the applicants respectfully submit that the rationale set forth in the official action for combining the cited references does not meet the requirements set forth in MPEP § 2143.

Therefore, the applicants respectfully submit that the rejection of claims 13 and 18 set forth in the official action does not comply with the requirements of MPEP § 2143 and respectfully request that the rejection be withdrawn.

5. Claims 15 and 20

Claims 15 and 20 are rejected under 35 USC § 103(a) as being unpatentable over Horiuchi as applied to Claims 11, 12, 16, and 17 in view of the Handbook. The applicants traverse the rejection on the grounds that the official action does not set forth a prima facie case of obviousness that complies with the requirements of MPEP § 2143.

First, the applicants respectfully submit that Horiuchi's device, modified as proposed in the official action, would still lack a mounting pad for the reasons set forth above with reference to claim 11. Accordingly, the applicants respectfully submit that the proposed combination of references does not teach or suggest every element of claims 15 and 20.

Second, the official action states:

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Wilson et al. with Horiuchi et al. to reduce costs (p. 868, lines 11 - 12) and reduce signal delays (p. 872, Figure 10).

As noted above, the cited passage of the Handbook describes the advantages of CVD tungsten in integrated circuits with three or more levels of metallization (p. 868, line 8). The substrate of Horiuchi's device package, on the other hand, has no more than two levels of metallization. Moreover, the portion of Horiuchi's device to which the official action proposes to apply the teachings of the Handbook is the substrate of a device package. The applicants respectfully submit that the substrate of a device package cannot accurately be described as an integrated circuit. Accordingly, the applicants respectfully submit that the person of ordinary skill in the art would regard the teaching set forth in the Handbook with respect to the material of the interlayer plugs of an integrated circuit

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with three or more levels of metallization as inapplicable to the choice of material of the vias of Horiuchi's device package. The applicants respectfully submit that such person would lack a motivation to make the combination of references proposed in the official action.

Referring to the motivations proposed in the official action, the applicants have been unable to find any teaching in the Handbook with regard to tungsten having a cost advantage in applications other than an integrated circuit with three or more levels of metallization. Finally, it is not clear from Figure 10 whether the data disclosed therein relates to interlayer plugs or to on-layer traces. The distance scales suggest the latter. Finally, it is not clear from Figure 10 that tungsten actually provides the advantage stated in the official action.

Accordingly, the applicants respectfully submit that the motivation set forth in the official action for combining the cited references does not meet the requirements set forth in MPEP § 2143.

Therefore, the applicants respectfully submit that the rejection of claims 15 and 20 is improper because the prima facie case of obviousness set forth in the official action does not meet the requirements set forth in MPEP § 2143. The applicants therefore respectfully request that the rejection be withdrawn.

6. Claim 19

Claim 19 is rejected under 35 USC § 103(a) as being unpatentable over Horiuchi as applied to Claims 11, 12, 16, and 17 in view of Moyer and Wyland. The applicants traverse the rejection on the grounds that the official action does not set forth a prima facie case of obviousness that complies with the requirements of MPEP § 2143.

First, the applicants respectfully submit that Horiuchi's device, modified as proposed in the official action, would still lack a mounting pad for the reasons set forth above with reference to claim 11. Accordingly, the applicants respectfully submit that the proposed combination of references does not teach or suggest every element of claims 15 and 20.

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Second, the official action states:

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Moyer et al. and Wyland with Horiuchi et al. to provide a metallic contact structures of low cost and high conductivity (Moyer et al., Col. 1, lines 41 -43).

The applicants respectfully submit that the prima facie case of obviousness set forth in the official action does not comply with the requirements of MPEP § 2143 because it does not propose a motivation for modifying Horiuchi's device package in accordance with the teaching of Wyland.

Moreover, as noted above, in the lines following the passage of Moyer's disclosure cited in the official action, Moyer discloses some of the many difficulties of using copper in integrated circuits. Moyer discloses a solution to the problems of using copper to form the bonding pads of an integrated circuit. Moyer's solution involves the deposition of several additional layers over the copper bonding pad. The applicants respectfully submit that the person of ordinary skill in the art would appreciate that the main motivation for adopting copper interconnects in integrated circuits, namely, maintaining low-resistance connections despite ever-decreasing feature sizes, does not apply to selecting the material of the pads of Horiuchi's device package. The applicants respectfully submit that this absence of a motivation to use copper, together with Moyer's teaching of the additional complexity of using copper, means that such person would have no motivation to adopt the teaching set forth in Moyer's disclosure with respect to the material of the pads of Horiuchi's device package.

Accordingly, the applicants respectfully submit that the rejection of claim 19 is improper because the prima facie case of obviousness set forth in the official action does not comply with the requirements of MPEP § 2143. The applicants therefore respectfully request that the rejection be withdrawn.

The applicants respectfully request reconsideration of the rejected claims. The applicants believe that the application as now amended is in condition for allowance, and respectfully request such favorable action. If any matters remain outstanding in the application, the Examiner is respectfully invited to telephone the applicants' attorney at (650) 485-3015 so that these matters may be resolved.

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Respectfully submitted,

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